SERIES 75450
DUAL PERIPHERAL DRIVERS

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT HIGH SPEEDS

performance

- 300-mA Output Current Capability
- High-Voltage Outputs
- High-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltages

SUMMARY OF DUAL DRIVERS

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGE
SN75450A	AND†	N
SN75451A	AND	P
SN75452	NAND	P
SN75453	OR	P
SN75454	NOR	P

†With transistor base connected directly to output of gate.

3

description

Series 75450 dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers. Additionally, the SN75450A may be used as a line driver. The SN75450A and SN75451A are functionally interchangeable with and are recommended for replacement of SN75450 and SN75451, respectively, in most applications which do not require the very high speed of the prototypes. The A-versions offer improved freedom from latch-up and diode-clamped inputs to simplify system design. They can drive lamps, relays, and memories to rated levels of voltage and current without external loading capacitors. Series 75450 drivers are monolithic circuits designed for operation over the temperature range of 0°C to 70°C.

The SN75450A is a unique general-purpose device featuring two standard Series 74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. The SN75450A offers the system designer the flexibility of tailoring the circuit to the application.

The SN75451A, SN75452, SN75453, and SN75454 are dual peripheral AND, NAND, OR, and NOR drivers respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN75450A	SN75451A SN75452 SN75453 SN75454	UNIT
Supply voltage, V_{CC}	7	7	V
Input voltage (see Note 1)	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	V
V_{CC}-to-substrate voltage	35		V
Collector-to-substrate voltage	35		V
Collector-base voltage	35		V
Collector-emitter voltage (see Note 3)	30		V
Emitter-base voltage	5		V
Output voltage (see Notes 1 and 4)		30	V
Continuous collector current (see Note 5)	300		mA
Continuous output current (see Note 5)		300	mA
Continuous total power dissipation	800	800	mW
Operating free-air temperature range	0 to 70	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.

recommended operating conditions (see note 6)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature range, T_A	0	25	70	°C

NOTE 6: For the SN75450A only, the substrate (pin 8), must always be at the most-negative device voltage for proper operation.

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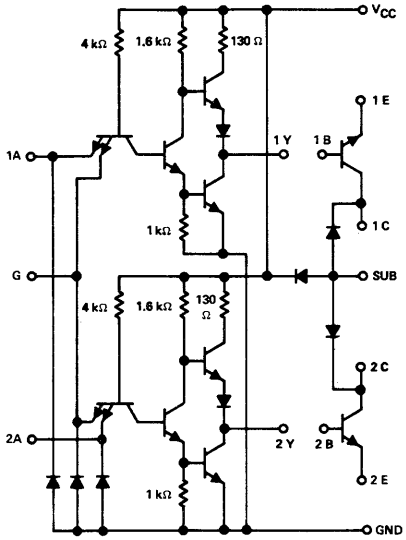
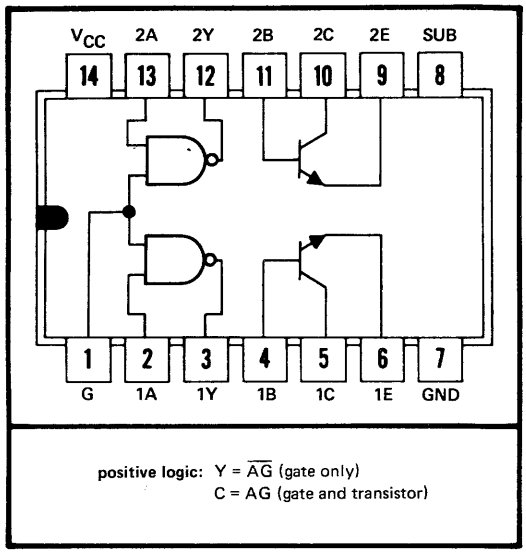
schematic



Component values shown are nominal

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		1		2			V
V_{IL}	Low-level input voltage		2				0.8	V
V_I	Input clamp voltage		3	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		2	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		V
V_{OL}	Low-level output voltage		1	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 16 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	input A	4	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
		input G					2	
I_{IH}	High-level input current	input A	4	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
		input G					80	
I_{IL}	Low-level input current	input A	3	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
		input G					−3.2	
I_{OS}	Short-circuit output current‡		5	V_{CC} = 5.25 V	−18		−55	mA
I_{CCH}	Supply current, high-level output		6	V_{CC} = 5.25 V, V_I = 0		2	4	mA
I_{CCL}	Supply current, low-level output			V_{CC} = 5.25 V, V_I = 5 V		6	11	mA

†All typical values at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA,	I_E = 0		35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA,	R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA,	I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, T_A = 25°C	I_C = 100 mA,	See Note 7	25			
		V_{CE} = 3 V, T_A = 25°C	I_C = 300 mA,		30			
		V_{CE} = 3 V, T_A = 0°C	I_C = 100 mA,		20			
		V_{CE} = 3 V, T_A = 0°C	I_C = 300 mA,		25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA,	I_C = 100 mA	See Note 7		0.85	1	V
		I_B = 30 mA,	I_C = 300 mA			1.05	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA,	I_C = 100 mA	See Note 7		0.25	0.4	V
		I_B = 30 mA,	I_C = 300 mA			0.5	0.7	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	12	C_L = 15 pF,	R_L = 400 Ω		20		ns
t_{PHL}	Propagation delay time, high-to-low-level output					8		ns

output transistors

PARAMETER		TEST FIGURE	TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
t_d	Delay time	13	I_C = 200 mA,	$I_{B(1)}$ = 20 mA,		8		ns
t_r	Rise time		$I_{B(2)}$ = −40 mA,	$V_{BE(off)}$ = −1 V,		12		ns
t_s	Storage time		C_L = 15 pF,	R_L = 50 Ω		7		ns
t_f	Fall time					6		ns

gates and transistors combined

PARAMETER		TEST FIGURE	TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	I_C = 200 mA,	C_L = 15 pF,		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output		R_L = 50 Ω			25		ns
t_{TLH}	Transition time, low-to-high-level output					10		ns
t_{THL}	Transition time, high-to-low-level output					12		ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

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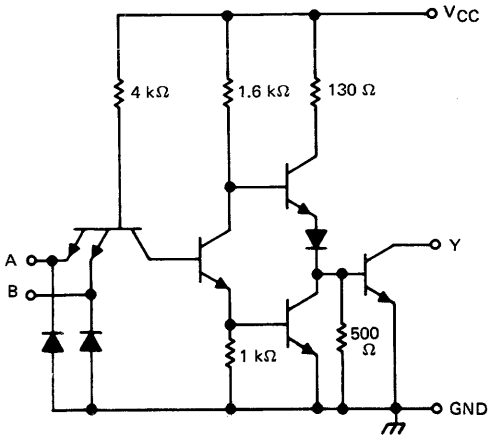
schematic (each driver)



Component values shown are nominal

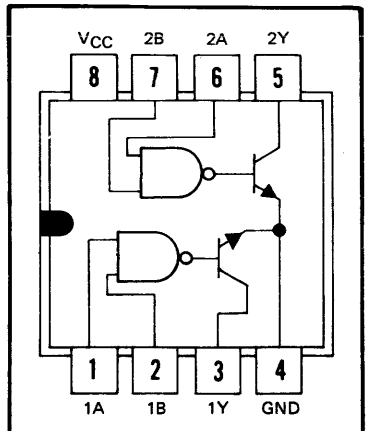
logic

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = high level, L = low level

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	10	V_{CC} = 5.25 V, V_I = 5 V		7	11	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 0		52	65	mA

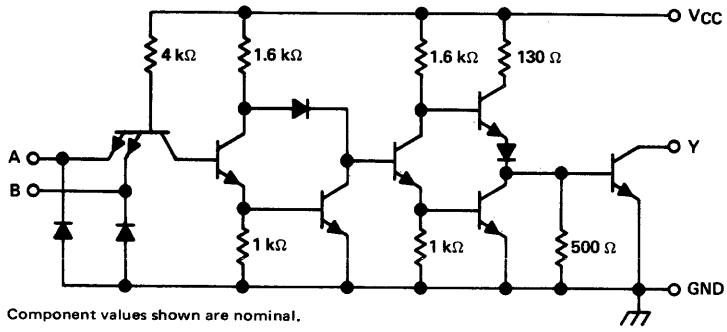
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

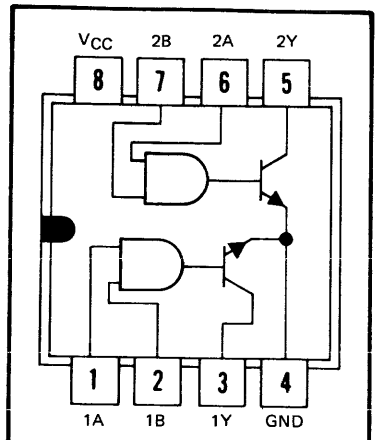
CIRCUIT TYPE SN75452
DUAL PERIPHERAL POSITIVE-NAND DRIVER

schematic (each driver)



Component values shown are nominal.

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

logic

3

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	10	V_{CC} = 5.25 V, V_I = 0 V		11	14	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 5 V		56	71	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output				35		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

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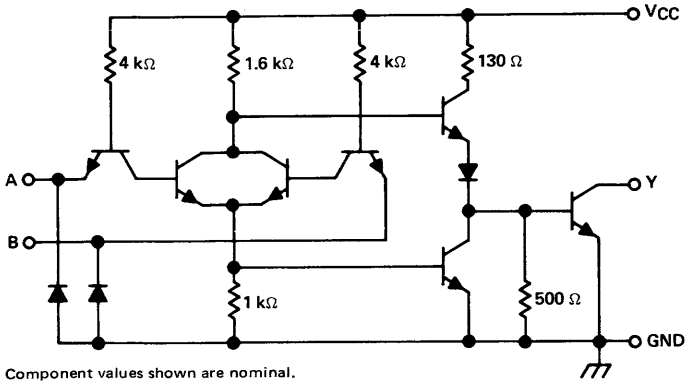
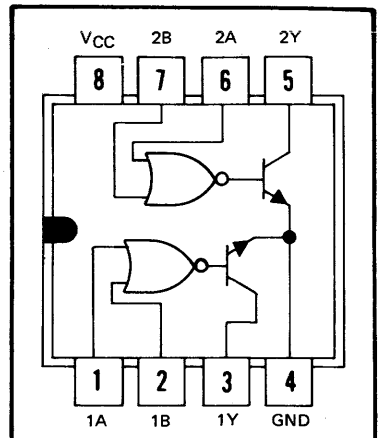
schematic (each driver)



Component values shown are nominal.

P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = A + B

logic

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = high level, L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	7	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	11	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 0		54	68	mA

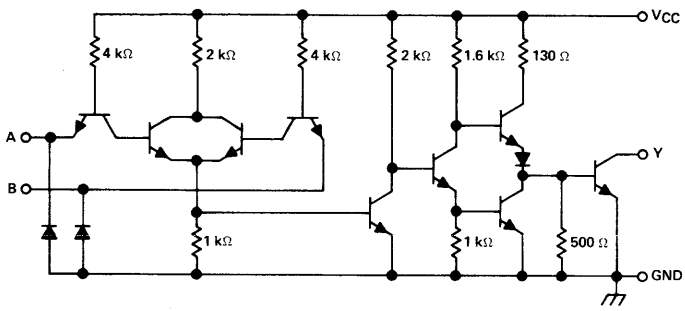
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		35		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

CIRCUIT TYPE SN75454
DUAL PERIPHERAL POSITIVE-NOR DRIVER

schematic (each driver)



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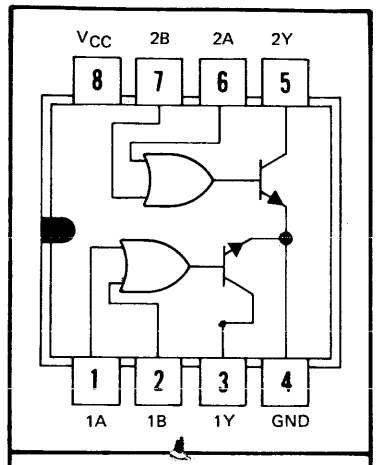
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A + B}$

3

logic

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = high level, L = low level

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	7		2			V
V_{IL}	Low-level input voltage	7				0.8	V
V_I	Input clamp voltage	8	V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_{OH}	High-level output voltage	7	V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{OH} = 30 V			100	μA
V_{OL}	Low-level output voltage	7	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	9	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	9	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	8	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, high-level output	11	V_{CC} = 5.25 V, V_I = 0 V		13	17	mA
I_{CCL}	Supply current, low-level output		V_{CC} = 5.25 V, V_I = 5 V		61	79	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output				25		ns
t_{TLH}	Transition time, low-to-high-level output				10		ns
t_{THL}	Transition time, high-to-low-level output				12		ns

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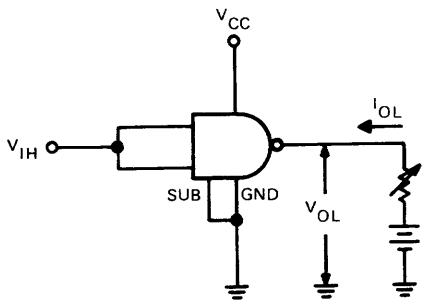
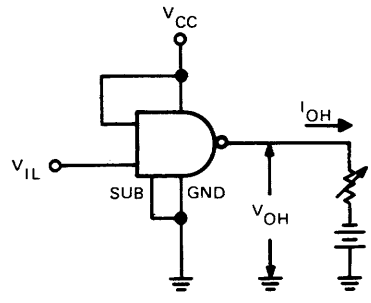
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †



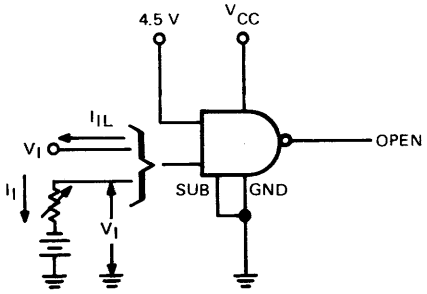
Both inputs are tested simultaneously.

FIGURE 1–V_{IH}, V_{OL}



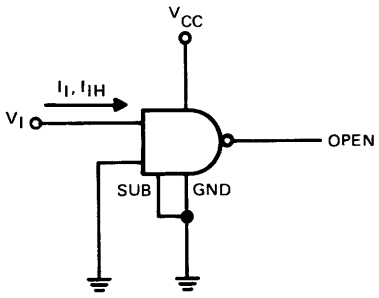
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



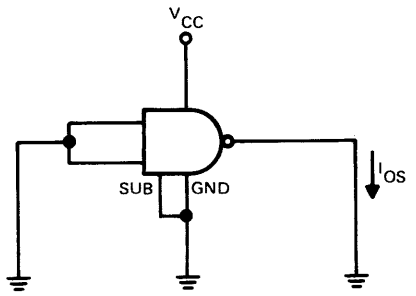
Each input is tested separately.

FIGURE 3–V_I, I_{IL}



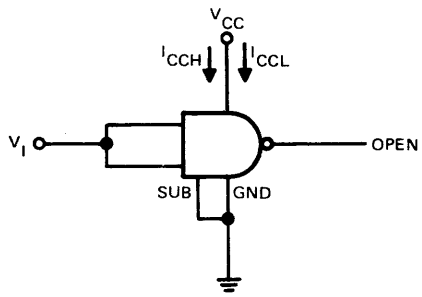
Each input is tested separately.

FIGURE 4–I_I, I_{IH}



Each gate is tested separately.

FIGURE 5–I_{OS}



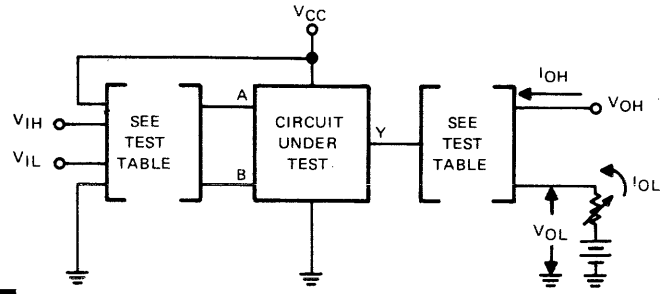
Both gates are tested simultaneously.

FIGURE 6–I_{CCH}, I_{CCL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

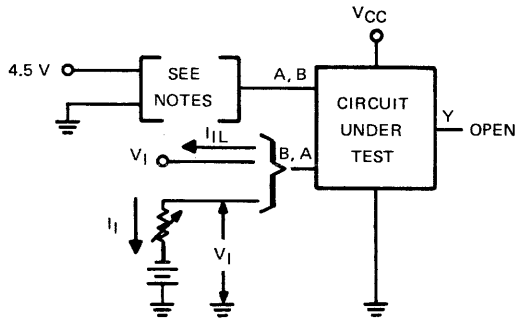


TEST TABLE

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
SN75451A	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
SN75452	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
SN75453	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
SN75454	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

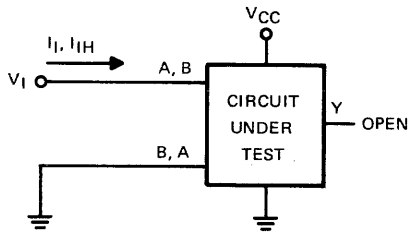
NOTE: Each input is tested separately.

FIGURE 7–V_{IH}, V_{IL}, I_{OH}, V_{OL}



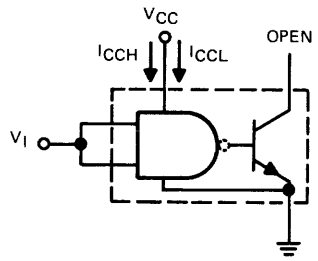
NOTES: A. Each input is tested separately.
B. When testing SN75453 and SN75454, input not under test is grounded. For all other circuits it is at 4.5 V.

FIGURE 8–V_I, I_{IL}



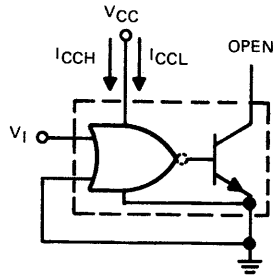
Each input is tested separately.

FIGURE 9–I_I, I_{IH}



Both gates are tested simultaneously.

FIGURE 10–I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

FIGURE 11–I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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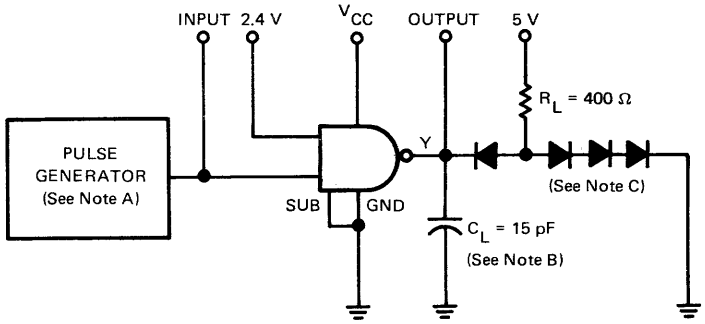
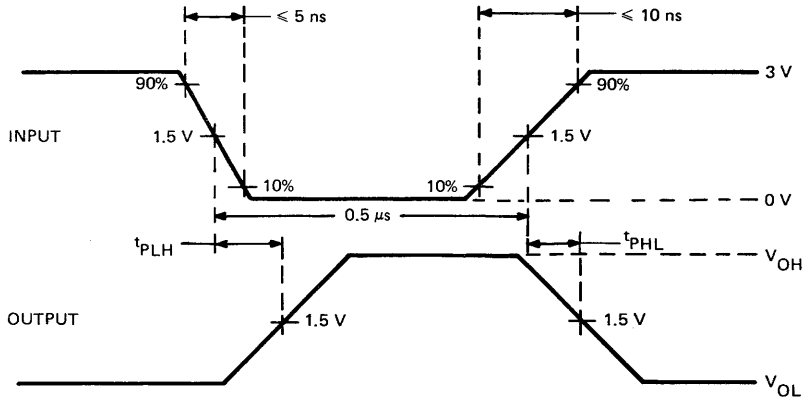
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



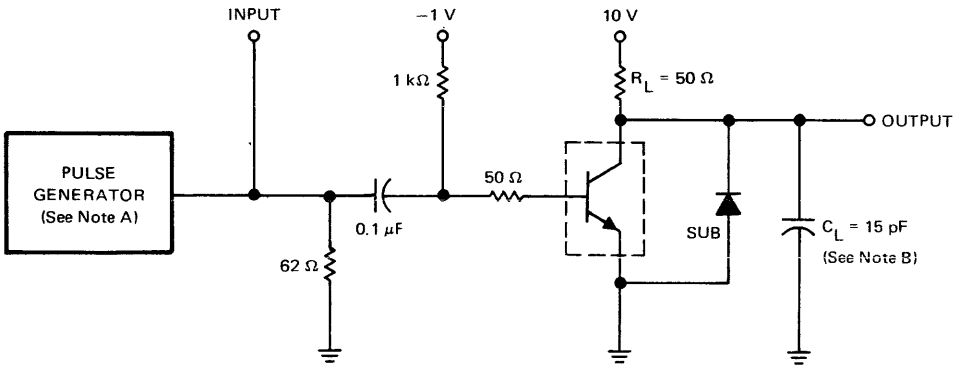
VOLTAGE WAVEFORMS

NOTES. A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

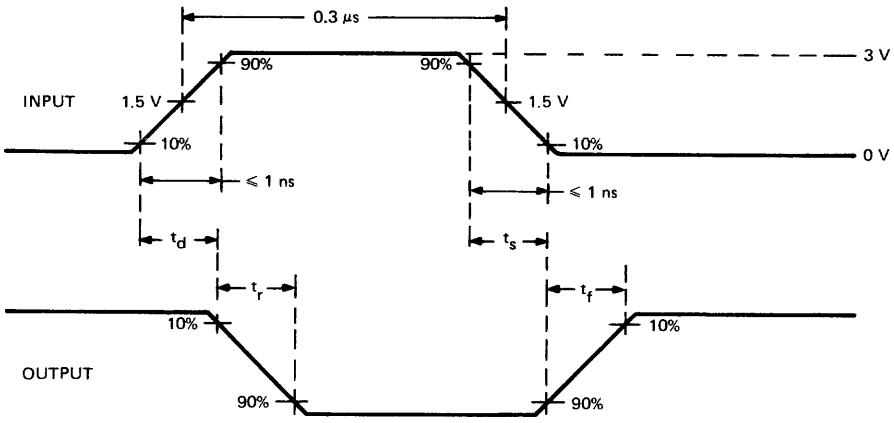
FIGURE 12–PROPAGATION DELAY TIMES, EACH GATE (SN75450A ONLY)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 13–SWITCHING TIMES, EACH TRANSISTOR (SN75450A ONLY)

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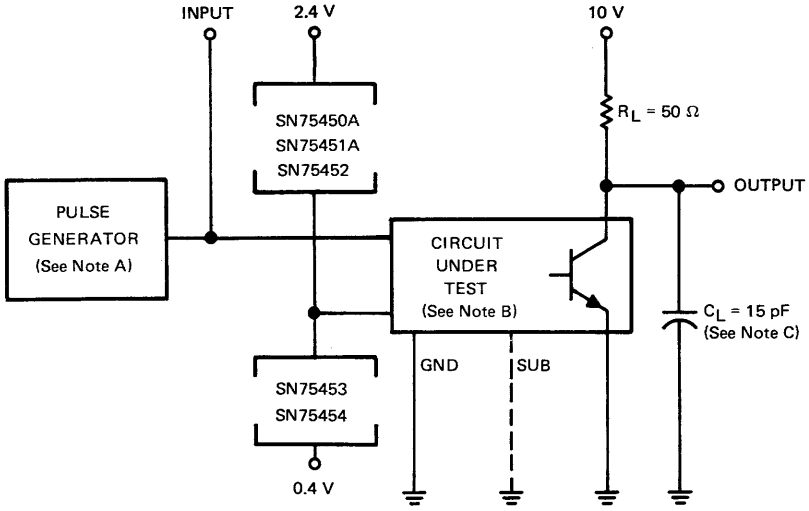
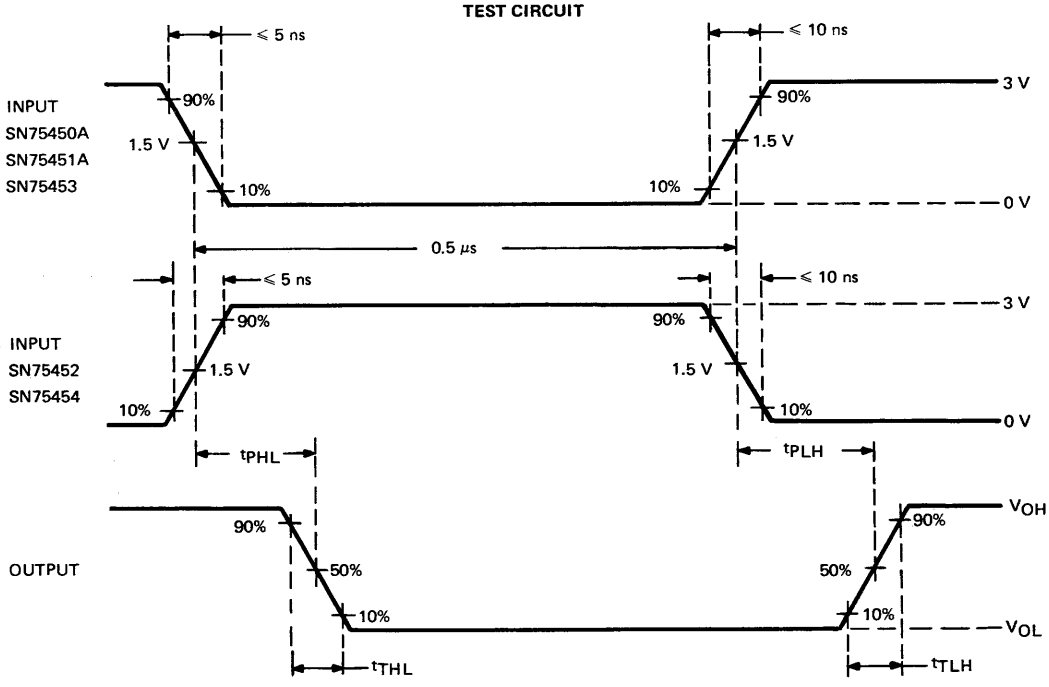
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing SN75450A, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 14–SWITCHING TIMES OF COMPLETE DRIVERS

TYPICAL CHARACTERISTICS

SN75450A
TTL GATE
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

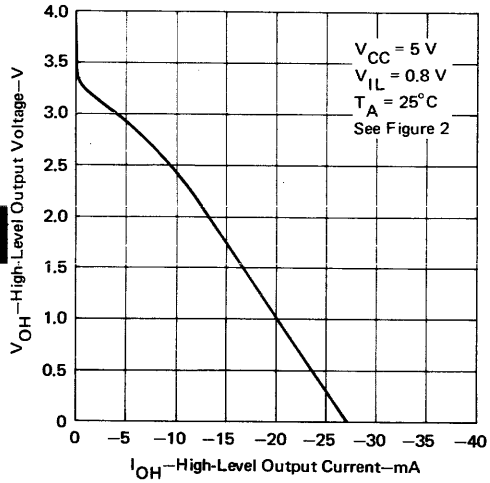


FIGURE 15

SN75450A
TRANSISTOR
STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

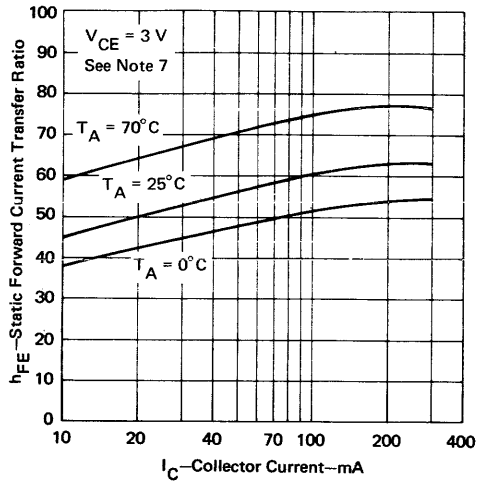


FIGURE 16

SN75450A
TRANSISTOR
BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

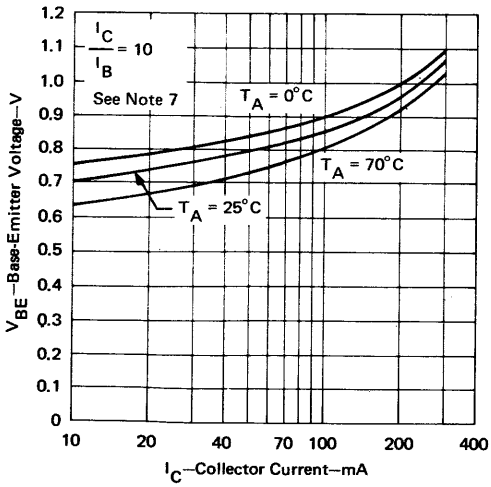


FIGURE 17

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

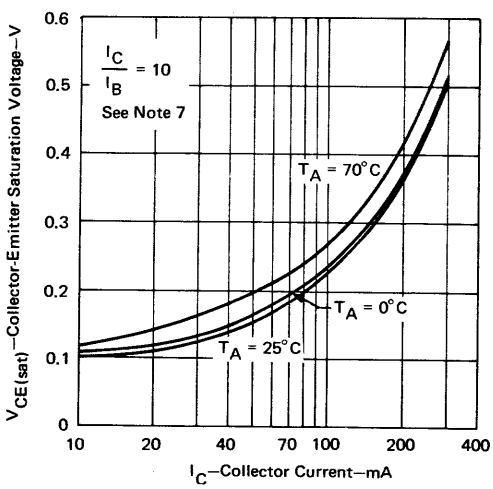
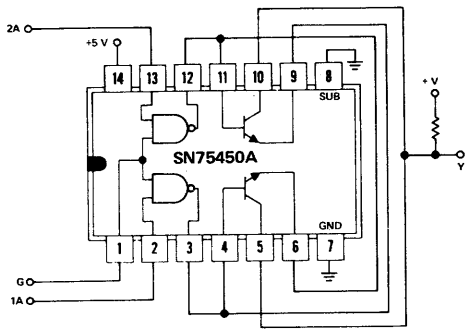


FIGURE 18

NOTE 7: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

TYPICAL APPLICATION DATA



$Y = \overline{G} + 1A \cdot 2A + 1\overline{A} \cdot 2\overline{A}$

FIGURE 19–GATED COMPARATOR

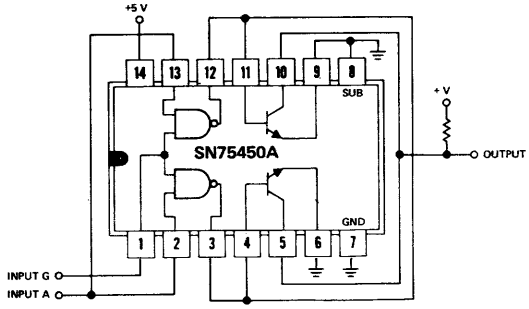


FIGURE 20–500-mA SINK

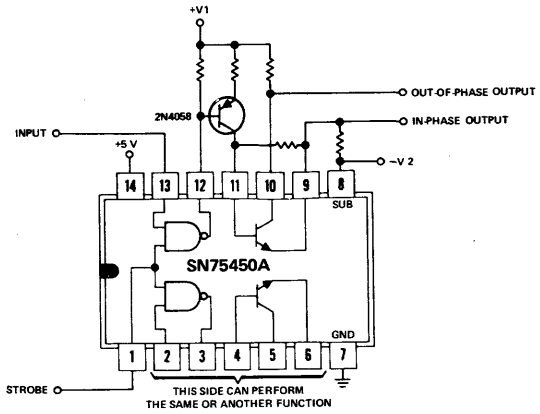


FIGURE 21–FLOATING SWITCH

TYPICAL APPLICATION DATA

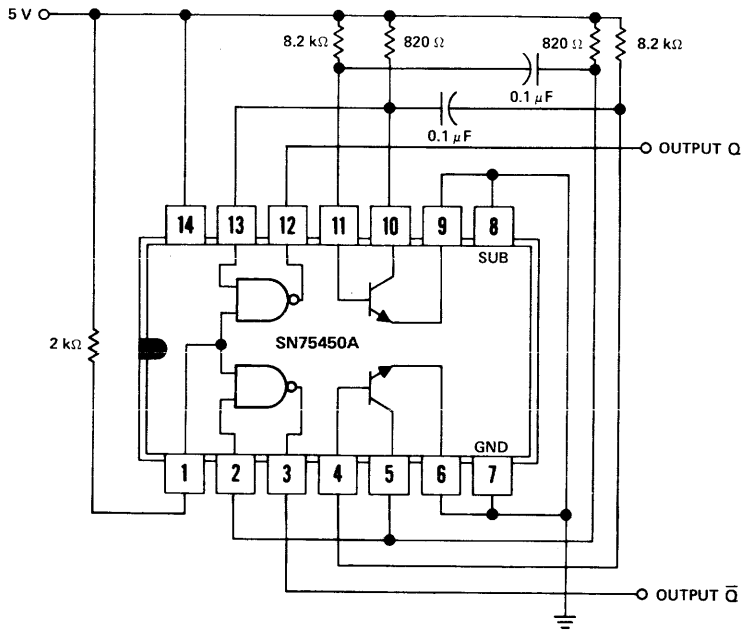
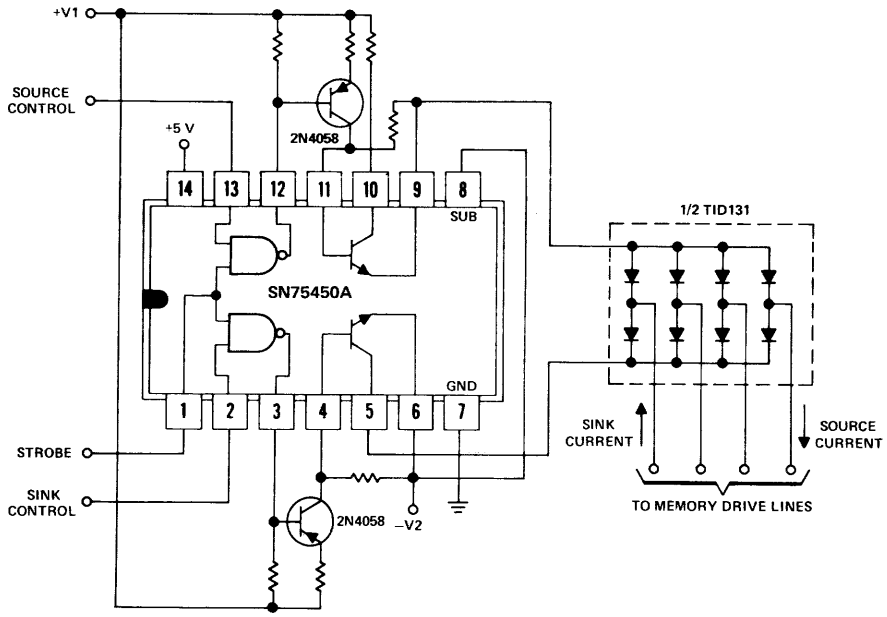


FIGURE 22–SQUARE-WAVE GENERATOR



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2V$).

FIGURE 23–CORE MEMORY DRIVER

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TYPICAL APPLICATION DATA

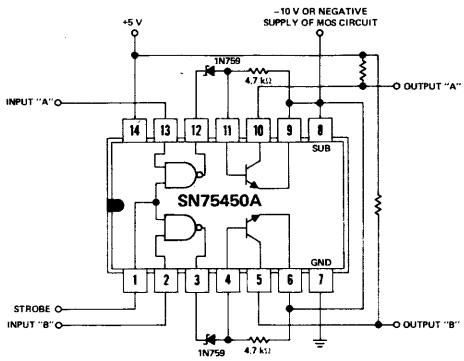


FIGURE 24—DUAL TTL-TO-MOS DRIVER

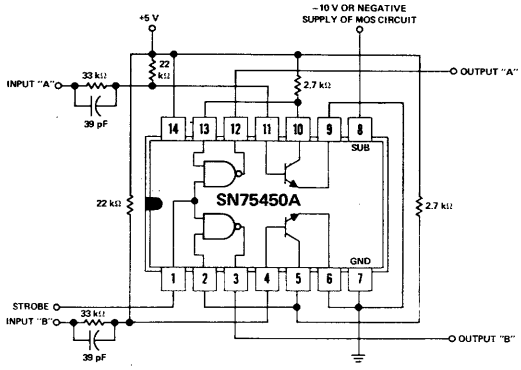
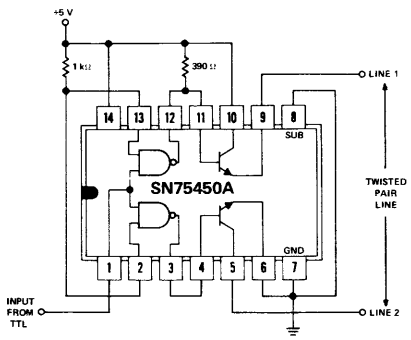
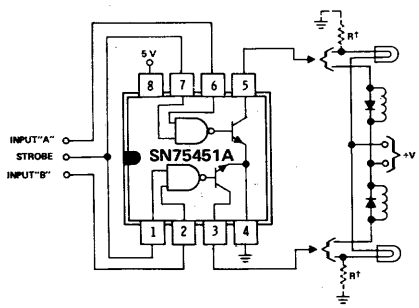


FIGURE 25—DUAL MOS-TO-TTL DRIVER



Termination is made at the receiving end as follows:
Line 1 is terminated to ground through $Z_O/2$;
Line 2 is terminated to +5 volts through $Z_O/2$;
where Z_O is the line impedence.

FIGURE 26—BALANCED LINE DRIVER



† Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

FIGURE 27—DUAL LAMP OR RELAY DRIVER

TYPICAL APPLICATION DATA

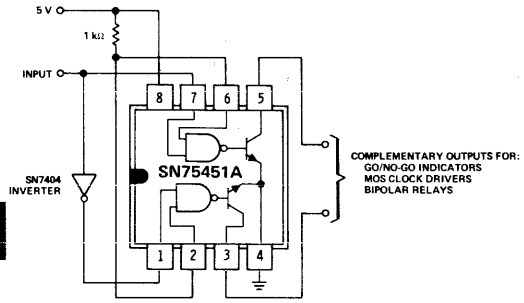


FIGURE 28–COMPLEMENTARY DRIVER

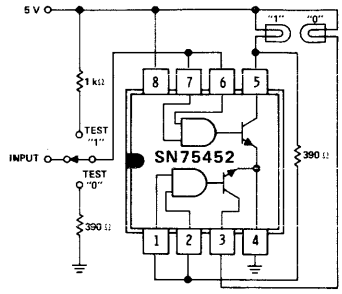
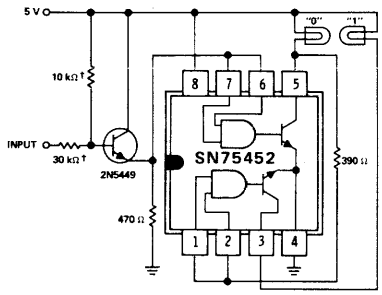


FIGURE 29–TTL OR DTL POSITIVE LOGIC-LEVEL DETECTOR



†The two input resistors must be adjusted for the level of MOS input.

FIGURE 30–MOS NEGATIVE-LOGIC-LEVEL DETECTOR

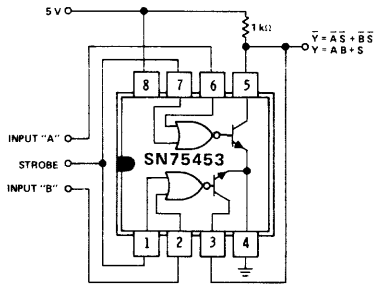


FIGURE 31–LOGIC SIGNAL COMPARATOR

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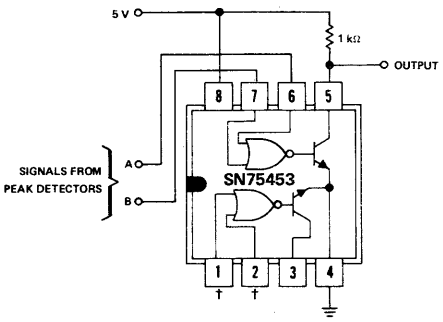
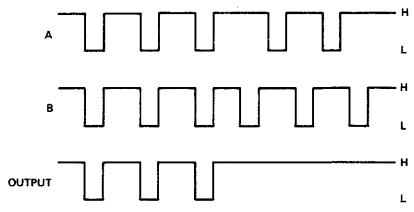
TYPICAL APPLICATION DATA





Low output occurs only when inputs are low simultaneously.

†If inputs are unused, they should be connected to +5 V through a 1 kΩ resistor.

FIGURE 32–IN-PHASE DETECTOR

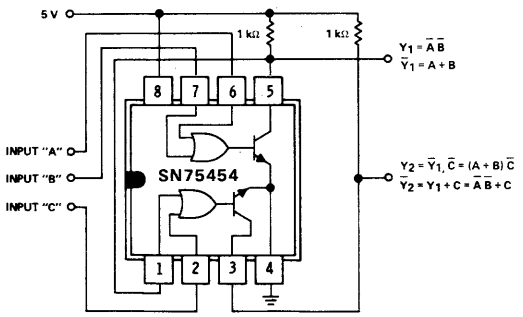


FIGURE 33–MULTIFUNCTION LOGIC-SIGNAL COMPARATOR

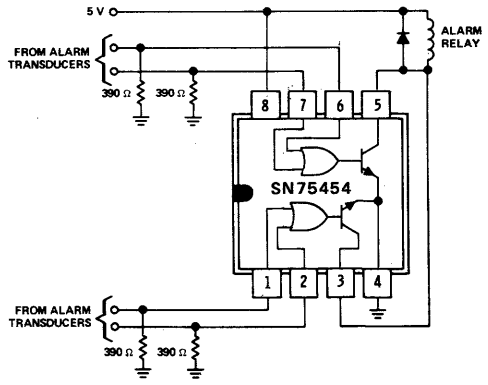


FIGURE 34–ALARM DETECTOR

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